REMARKS/ARGUMENTS

Examiner Nguyen is thanked for the thorough examination of the subject Patent Application. The Claims have been carefully reviewed and amended, and are considered to be in condition for allowance.

Reconsideration of the objection to the amendment filed 1/14/05 under 35 U.S.C. §132 because it introduces new matter into the disclosure of the invention. The applicant believes that added material is not new matter. The original text describes that:

"Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage..." (Page 5, last paragraph, lines 2-4)

Employing basic electronic principles, the large coupling ratio provides a charge coupling or AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. Thus the coupling ratio would be defined as:

$$CR = \frac{VB11}{VSS} = \frac{VSS\frac{Z_{CP}}{Z_{HC}+Z_{CP}}}{VSS} = \frac{Z_{CP}}{Z_{HC}+Z_{CP}}$$

$$= \frac{\frac{1}{j\omega C_P}}{\frac{1}{j\omega C_{HC}}+\frac{1}{J\omega C_{HC}}} = \frac{C_{HC}}{C_{HC}+C_P}$$

Where:

$$Z_{CP} = \frac{1}{j\omega C_P},$$

$$Z_{HC} = \frac{1}{J\omega C_{HC}}, \text{ and}$$

$$VB11 = V_{CP} = VSS\frac{Z_{CP}}{Z_{HC} + Z_{CP}}.$$

It can be shown that as the magnitude of the capacitance of the large capacitor $\mathbf{C_{HC}}$ relative to the capacitance of the parasitic capacitor $\mathbf{C_P}$ grows larger, any noise voltage present on the lower supply voltage VSS is charge coupled or AC coupled directly to the bias node **b11**. Further it is apparent that the larger magnitude of the capacitance of the large capacitor $\mathbf{C_{HC}}$ relative to the capacitance of the parasitic capacitor $\mathbf{C_P}$, the coupling ratio approaches a maximum value of unity (1), therefore a large coupling value would clearly be any value that approached unity (1).

The applicant requests that the clean version of the specification as presented in the appendix of the amendment of June 29, 2005 be entered as conforming to 37 CFR 1.125(b) and (c). As explained in detail above, the specification contains no new matter. The clean version of the specification as

presented in this amendment shows the amendment to the specification and the Claims as shown above.

Reconsideration of the objection to Claims 1-42 because of informalities is requested. Claims 1-42 are amended to provide correct description of the elements and function of the elements as requested by the Examiner.

Reconsideration of the rejection under 35 USC §112, first paragraph of Claims 1-42 for failing to comply with the written description requirements, in that the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor at the time of the application was filed, had possession of the claimed invention is requested in light of the following arguments.

The original text describes that:

> "Because of its large coupling ratio, CHC essentially charge couples the VB11 gate voltage of the PMOS bias node, to the VSS source voltage..." (Page 5, last paragraph, lines 2-4)

Employing basic electronic principles, the large coupling ratio provides a charge coupling or AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. Thus the coupling ratio would be defined:

$$CR = \frac{VB11}{VSS} = \frac{VSS\dfrac{Z_{CP}}{Z_{HC}+Z_{CP}}}{VSS} = \frac{Z_{CP}}{Z_{HC}+Z_{CP}}$$

$$= \frac{\dfrac{1}{j\omega C_P}}{\dfrac{1}{j\omega C_{HC}}+\dfrac{1}{j\omega C_{HC}}} = \frac{C_{HC}}{C_{HC}+C_P}$$

Where:

$Z_{CP} = \dfrac{1}{j\omega C_P}$ is the impedance of the parasitic capacitance C_P.

$Z_{HC} = \dfrac{1}{j\omega C_{HC}}$ is the impedance of the very large capacitance C_{HC}.

$VB11 = V_{CP} = VSS\dfrac{Z_{CP}}{Z_{HC}+Z_{CP}}$ is the voltage VB11 present at the node b11 and can be found as a voltage divider of the impedance Z_{HC} of the very large capacitor C_{HC} and the impedance Z_{CP} of the parasitic capacitor C_P as shown.

It can be shown that as the magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P grows larger, any

noise voltage present on the lower supply voltage VSS is charge coupled or AC coupled directly to the bias node b11. Further it is apparent that the larger magnitude of the capacitance of the large capacitor C_{HC} relative to the capacitance of the parasitic capacitor C_P, the coupling ratio approaches a maximum value of unity (1), therefore a large coupling value would clearly be any value that approached unity (1).

The concept of coupling ratio is not new in the art, as shown in Silicon Processing for the VLSI Era, Volume II Process Integration, Wolf, Latice Press, Sunset Beach, CA., 1990, pp: 623-627. In nonvolatile or Flash memory, the capacitive coupling coefficient of the capacitance of the control gate to the floating gate of the nonvolatile memory cell and the capacitance of the floating gate of the nonvolatile memory cells to the bulk semiconductor substrate of a nonvolatile memory cell, the coupling coefficient is used to determine the amount of charge coupled to the floating gate to determine the necessary programming voltages and the time for programming the nonvolatile memory cell. The serial structure of the floating gate nonvolatile memory employs similar concepts to the present invention. The very large capacitor C_{HC} in series with the parasitic capacitor C_P as shown in Fig. 4a demonstrates that the large value of capacitance of the very large capacitor C_{HC} relative to the parasitic capacitor C_P causes the voltage VB11 at the node b11 is essentially equal to the lower supply voltage VSS and the coupling ratio approaches one (1) as shown above.

Reconsideration of the rejection under 35 USC §112, second paragraph, of Claims 1-42 as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention is requested in light of the following arguments.

In Claims 1, 12, 23, and 33, a large capacitor is coupled between the bias node and the lower supply voltage:

> "for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point."

As shown in Silicon Processing for the VLSI Era, Volume II Process Integration, Wolf, Latice Press, Sunset Beach, CA., 1990, pp: 623-627, the coupling ratio is not the ratio of the value of capacitance between the very large capacitor C_{HC} and parasitic capacitor C_P (C_{HC}/C_P), but the AC coupling of the biasing voltage VB11 at the bias node b11 to the lower supply voltage VSS. This is essentially a

capacitive voltage divider and as shown above, the voltage VB11 at the bias node b11 become a function of the coupling ratio ($\frac{C_{HC}}{C_{HC} + C_P}$).

Reconsideration of the rejection under 35 USC §103(a) of Claims 1-42 as being unpatentable over in Applicant's Admitted Prior Art (AAPA) in view of U. S. Patent 6,373,328 (Rapp) is requested in light of the following arguments.

The AAPA does illustrate an input buffer receiver and Rapp does show "an n-type transistor 90" connected to serve "as a capacitor, helping to hold the voltage constant at the gate of transistor 86" (Rapp, Col 9, Lines 38-42). Neither AAPA, nor Rapp, nor AAPA in combination with Rapp include:

> a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; (Claim 1, Lines 4-11 and Claim 12, Lines 7-17)

> forming a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of

said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point; (Claim 23, Lines 6-13)

and

means for forming a large capacitor between the bias node and the lower supply voltage for providing a coupling ratio between a capacitance value of said large capacitor and a capacitance value of a parasitic capacitor coupled between said bias node and a ground reference point is approximately equal to a unity value such that a biasing voltage at said biasing node follows said lower supply voltage to minimize effects of said ground noise between the lower supply voltage and the ground reference point. (Claim 33, Lines 8-15)

The large capacitor in Rapp is connected to the ground reference point and does not charge couple the biasing node to the lower supply voltage such that the voltage at the biasing node follows the lower supply voltage. Further, the circuit of Rapp provides a comparator circuit that compares the voltage value of a programming voltage supply V_{PP} at node A of Fig. 5 of Rapp against the voltage

value of the power supply voltage V_{DD}. The capacitor of Rapp helps "to hold the voltage constant at the gate of transistor 86" this does not provide the coupling of the lower supply voltage to the biasing node of this invention.

The invention as claimed in amended Claims 1-42 is believed to be novel and patentable over AAPA in view of Rapp because there is not sufficient basis for concluding that claimed elements of either AAPA, or Rapp, or AAPA in combination with Rapp would have been obvious to one skilled in the art. That is to say, there must be something in the prior art or line of reasoning to suggest that the combination of these various references is desirable. The applicant believes that there is no such basis for the combination. The applicant, therefore, request Examiner Nguyen reconsider his rejection in view of these arguments.

It is requested that should Examiner Nguyen not find that the Claims are now allowable, that the undersigned be called at (845) 452-5863 to overcome any problems preventing allowance.

Respectfully Submitted,
George O. Saile & Associates

Billy J Knowles

Billy J. Knowles, Reg. No. 42,752
Telephone: (845) 452-5863